IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Appl. No.	:	TBD	Confirmation No. TBD
Applicant	:	Chiu et al.	
Filed:	:	Herewith	
TC/A.U.	:	TBD	
Examiner	:	TBD	
Docket No.	:	TI-34032A	
Customer No.	:	23494	

Mail Stop Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO Form 1449. Pursuant to the new rules, only copies of the non - U.S. Patents and Publications listed are enclosed.

Please charge any fees due in connection with the filing of this paper to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. Please credit any excess fees to the same deposit account.

Respectfully submitted,

Texas Instruments Incorporated
P. O. Box 655474 MS 3999
Dallas, Texas 75265
(972) 917-5355

Yingsheng Tung
Attorney for Applicant(s)
Reg. No. 52,305

FORM PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*	**TI-34032A**	**TBD**
	APPLICANT: **Chiu et al.**	
	FILING DATE **Herewith**	GROUP **TBD**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		US 6,385,049 B1	05/07/02	Chia-Yu et al.	361	721	07/05/2001
		5,879,792	03/09/99	Watanabe et al.	428	304.4	01/13/1997
		5,709,146	01/20/98	Watanabe	101	128.21	03/29/1996
		US 6,213,347 B1	04/10/01	Thomas	222	52	04/30/1999
		US 6,228,680 B1	05/08/01	Thomas	438	108	05/01/1999
		US 6,245,583	06/12/01	Amador et al.	438	14	04/30/1999

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER NON-PATENT DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		"Flip-Chip On Film Assembly for Ball Grid Array Packages" Coyle et al., U. S. Patent Publication No. US 2002/0084521 A1, Published 4 July 2002
		"Flexible Ball Grid Array Chip Scale Packages and Methods of Fabrication", Moon et al. U. S. Patent Publication No. US 2002/0164838 A1, Published 7 Nov., 2002
		"Plastic Chip-Scale Package Having Integrated Passive Components", Pritchett et al., U. S. Patent Publication No. US 2002/0015292 A1, Published 7 Feb., 2002
		"SLT Device Metallurgy and its Monolithic Extension", Totta et al., IBM J. Res. Develop. May, 1969, pp. 226-238
		"Controlled Collapse Reflow Chip Joining", Miller, IBM Components Division, Fishkill New York, May 1969, pp. 239-250
		"Geometric Optimization of Controlled Collapse Interconnections", Goldmann, IBM Components Division, Fishkill, New York, May 1969, pp. 251-265
		"Reliability of Controlled Collapse Interconnections", Norris et al., IBM J. Res. Develop. May 1969, pp.-266-271
		"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Oktay, IBM J. Res. Develop., May 1969, pp. 272-285
		"Studies of the SLT Chip Terminal Metallurgy", Berry et al, IBM J. Res. Develop. May 1969, pp. 286-296
		"Parallel Methods for Approximating the Root of a Function", Miranker, IBM Watson Research Center, Yorktown Heights, New York, May 1969 pp. 297
		"Chip Scale Package (CSP)", Lau et al, McGraw Hill
		"Effect of Simulation Methodology on Solder Joint Crack Gr wth Correlation", Darveaux, IEEE Electronic Components and Technology C nference, 2000, pp. 1048-1058
		"Reliability of Plastic Ball Grid Array Assembly, Darveaux, et al, Chapter 13

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.